

Notice of References Cited	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10/078,180	MORROW, NEIL G.
	Examiner	Art Unit
	Thomas J. Cleary	2111
		Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,802,324 A	09-1998	Wunderlich et al.	710/300
*	B	US-6,070,214 A	05-2000	Ahern, Frank	710/315
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"Free On-Line Dictionary of Computing", entry 'High Performance Serial Bus'. [posted 3 Sep 2000]. [retrieved 27 Apr 2004]. < http://foldoc.doc.ic.ac.uk/foldoc/foldoc.cgi?query=1394 >
	V	"Low Pin Count (LPC) Interface Specification", Revision 1.0 [29 Sep 1997]. Intel Corporation. Chapter 1, Page 1.
	W	"Time Budgeting of the FlatLink Interface", Application Report [June 1997]. Kevin Gingerich. Texas Instruments Incorporated.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.